DATA BUFFER-CONTROLLED DIGITAL CLOCK REGENERATOR

ABSTRACT

A clock regeneration scheme for a digital communication receiver has a first-in, first-out (FIFO) storage buffer into which received data is clocked in accordance with an input clock signal and a data valid signal. A fixed fractional delay line is coupled to provide respectively different phase delayed versions of the input clock signal and feeds a multiplexer that is controllably operative to couple one of the outputs of the fixed fractional delay line to a regenerated clock output port. A control loop, which includes the FIFO storage buffer, the output port and a steering control input of the multiplexer circuit, is operative to selectively change which output of the fixed fractional delay line is coupled by the multiplexer to the output port, so as to controllably cause the output clock signal to track the effective frequency of the valid data signal.